

The Symposium on Polymers for Microelectronics
Winterthur Museum & Gardens, Copeland Lecture Hall
12th Meeting Preliminary Agenda
May 3-5, 2006

Wednesday, May 3

7:30-5:00pm REGISTRATION at Winterthur Pavilion

8:25-8:30am Opening Remarks

SESSION I **BUFFER COATING APPLICATIONS**

SESSION CHAIRS: Ed Prack, Intel / Jack Craig, PI Consul

8:30-9:15am

Keynote Address

Challenges and Requirements in Buffer Coating Process, J.H. Kim, Samsung Electronics, Korea

9:15-9:40am

Wafer Level Stress Buffer Layer Processing as a Cost-Effective Means of Increasing the Yield of Precision Analog Parts, D. Crenshaw et al, Texas Instruments, Dallas, TX

9:40-10:05am

Aqueous Developable, Negative-Tone Buffer Coat Material, I. Rushkin and D. Racicot, FUJIFILM Electronic Materials, North Kingstown, RI

10:05-10:30am

Break

10:30-10:55am

HD4004 PSPI Manufacturing Integration and CPI Qualification, R. Volant et al, IBM, East Fishkill, NY

10:55-11:20am

Development of aqueous developable negative type photosensitive polyimide, K. Katoh, HD Microsystems, Ibaraki, Japan

11:20-11:45am

Chemically Amplified Photodefinable Poly(benzoxazole) Using Dissolution Reversers, T. Minegishi et al, Hitachi Chemical, Ibaraki, Japan

11:45-12:10pm

Photosensitive Polyimide: Selecting Positive or Negative Tone?, J. Reche, Optomag, Tempe, AZ

12:10-1:40pm

Lunch, Winterthur Pavilion

SESSION II

STRUCTURE PROPERTY RELATIONSHIPS AND CHARACTERIZATION

SESSION CHAIRS: Sue Ann Bidstrup-Allen, Georgia Tech / Paul Ho, University of Texas

1:40-2:05pm

Underfill Design for High Density Interconnect (HDI) Flip-Chip Packages, E. Dimotakis et al, Intel, Chandler, AZ

2:05-2:30pm

Characterizing Molded Package Stress Utilizing Tensile Modulus Measurements, A. Shoenberg, Fairchild Semiconductor, South Portland, ME

2:30-2:55pm

Fabrication of a Tensile Test for Polymer Micromechanics, U. Lang and J. Dual, IMES – Center of Mechanics, ETH Zurich, Switzerland

2:55-3:20pm

Terahertz and Millimeter Wave Properties of Dielectrics for Electronic Applications, J. Dougherty et al, Pennsylvania State University, Freeport, PA

3:20-3:45pm

Break

3:45-4:10pm

Investigation of Die Attach Film Adhesive Delamination By Thermomechanical Analysis, L. Buenaflor and S. Dal, Intel, Cavite, Philippines

4:10-4:35pm

Low Temperature Curing of Polybenzoxazole (PBO) Films on Wafers, R. Hubbard et al, Lambda Technologies / HD Microsystems, Mesa, AZ

4:35-5:00pm

Plasma treatment study of Polyimide to ACF for adhesion improvement, Y. Kaneya et al, HD Microsystems, Ibaraki, Japan

5:30-7:00 pm

Symposium Reception, Reflecting Pool, Winterthur Mansion

Thursday, May 4

8:00-8:05am Opening Remarks

SESSION III **FRONT-END OF LINE APPLICATIONS**

SESSION CHAIRS: Mike Goodner, Intel / John Malloy, HD Microsystems

8:05-8:50am

Keynote Address

Polymers as Low-k Dielectrics for Integrated Circuits; Challenges and Opportunities, J. Gambino, IBM Microelectronics, Essex Junction, VT

- 8:50-9:15am **Polycarbosilanes As Low-K Dielectric Materials**, L. Interrante et al, Rensselaer Polytechnic Institute, Troy, NY
- 9:15-9:40 am **Novel Siloxane Polymers for FEOL Applications**, R. Ghoshal, Polyset Company, Mechanicville, NY
- 9:40-10:05am **Preorganization in Photoresist Architecture**, R. Meagley et al, Intel and Lawrence Berkeley National Laboratory, Berkeley, CA
- 10:05-10:30am **Optimizing the Vapor Deposition Method of Making Polyimide**, A. Knight et al, University of Rochester, Rochester, NY
- 10:30-10:55am **Break**
- SESSION IV** **BACK-END OF LINE APPLICATIONS**
- SESSION CHAIRS: Tim Daubenspeck, IBM / Bill Motsiff, WMC
- 10:55-11:20am **Future Trends and Drivers for IC Packaging and the Impact on Materials**, E. Vardaman, TechSearch International, Austin, TX
- 11:20-11:45am **Current and Future Trends in Wafer Level Packaging**, T. Tessier et al, FlipChip International, Phoenix, AZ
- 11:45-12:10pm **Polymer-based Wafer-Level Packaging of MEMS**, P. Joseph et al, Georgia Institute of Technology, Atlanta, GA
- 12:10-1:40pm **Lunch**, Winterthur Pavilion
- 1:40-2:05pm **WLCSP Materials: Science and Alchemy**, J. Hunt and W. Chen, ASE, Tempe, AZ
- 2:05-2:30pm **The Role of Thin Film Polymers in SiP Applications**, M. Töpper et al, Fraunhofer IZM Berlin / Technical University of Berlin, Berlin, Germany
- 2:30-2:55pm **Underfill to Die Passivation Adhesion Testing**, M. Gaynes et al, IBM, Yorktown Heights, NY
- 2:55-3:20pm **Void Formation Mechanism in an Epoxy/polyimide Film Adhesive**, S. Dal, Intel, Cavite, Philippines
- 3:20-3:45pm **Break**
- 3:45-4:10pm **Designing Underfill Material in Resolving Package High Coplanarity Issues**, B. Yam, Intel, Penang, Malaysia
- 4:10-4:35pm **Pre-applied Underfills for Lead-free Flip Chip**, R. Mills, General Electric, Niskayuna, NY
- 4:35-5:00pm **Molding Underfill Material Development for High Performance FCBGA**, W. Lee et al, Siliconware Precision Industries, Taichung, Taiwan, R.O.C
- 6:00-9:30pm **Symposium Exhibitors, Cocktails and Dinner**, DuPont Country Club, Rockland, DE

Friday, May 5

- 8:00-8:05am Opening Remarks
- SESSION V** **EMERGING AND NOVEL APPLICATIONS**
- SESSION CHAIRS: Ray Fillion, GE / Robb White, SAIC
- 8:05-8:50am **Keynote Address**
Emerging Applications of Inherently Conductive Polymers, M. Aldissi, Fractal Systems, Safety Harbor, FL
- 8:50-9:15am **Laser Direct Write Termination of Ultra-miniature Chip Resistors Using a Non-Photosensitive Resist**, E. Swenson and R. Shick, ESI / Promerus Electronic Materials, Portland, OR
- 9:15-9:40am **Printed Electronics Utilizing Ink Jet Technology**, D. Hayes, MicroFab Technologies, Plano, TX
- 9:40-10:05am **Optical Component Coupling using Self-aligned Polymeric Waveguide Interconnection**, T. Gorczyca et al, GE Global Research, Niskayuna, NY
- 10:05-10:30am **Break**
- 10:30-10:55am **High Capacitance, Large Area, Thin Film, Nanocomposite Based Embedded Capacitors Integration of High Dk Polymeric Nanocomposites in Microelectronics**, M. Poliks et al, Endicott Interconnect Technologies, Endicott, NY
- 10:55-11:20am **Embedded Actives and Passives for System-on-Package Applications**, R. Fillion et al, GE Global Research, Niskayuna, NY
- 11:20-11:45am **(Flat) Ultra-Thin Chip Package**, W. Christiaens and J. Vanfleteren, Ghent University, Ghent Belgium
- 11:45am **Adjorn**