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AGENDA

THE FOURTEENTH MEETING OF THE SYMPOSIUM ON POLYMERS FOR MICROELECTRONICS

MAY 11, 12, & 13, 2010



Winterthur Museum & Gardens
Copeland Lecture Hall
Wilmington, Delaware

The Symposium on Polymers for Microelectronics
 Winterthur Museum & Gardens, Copeland Lecture Hall
14th Meeting Agenda
 May 11-13, 2010

Tuesday **Session 1 - Wafer and Embedded**
May 11, 2010 **IC Packaging**

- 8:30 **Welcome; Symposium Opening Remarks**
- 8:35 Chip Package Interaction **Jon Casey**
 IBM Systems and
 Technology Group,
- 9:20 Impact of Chip-Packaging
 Interaction on Interfacial
 Cracking of Multilevel
 Cu/Low-k Interconnect
 Structures **Paul Ho**
 University of Texas
- 9:45 Chip-Package Interaction **Timothy Daubenspeck**
 (CPI) and Chip Level Final
 Via Design IBM
- 10:10 Polymer Requirements for
 Advanced Wafer Level
 Packaging **John Hunt**
 ASE,
- 10:35 - 11:00 **Break**
- 11:00 Polymer Nanocomposite
 Based Embedded Passives
 Towards System in
 Package (SiP) **Susan Bagen**
 Endicott Interconnect
 Technologies, Inc.
- 11:25 Development of a Low
 Temperature Curing -
 Aqueous Base Developable
 Photoimageable Dielectric
 for WLP (Wafer Level
 Packaging) Applications **Michael Gallagher**
 Dow Electronic
 Materials
- 11:50 Reduced Moisture Uptake
 and Moisture Expansion
 Polyimides **Garrett D Poe**
 NeXolve
- 12:15 - 1:30 **Lunch**
- 1:30 Ultra Low Temperature
 Curable Positive Tone
 Photodefineable
 Polybenzoxazole **Tomonori Minegishi**
 Yamazaki R&D Center,
 HD Microsystems, Ltd
 and Hitachi Chemical Co.
- 1:55 Design of Novel Positive
 Tone Photosensitive
 Polyimide with High
 Sensitivity and Accurate
 Pattern Fidelity **Masao Tomikawa**
 Toray Industries
- 2:20 Cross-linking of Aqueous-
 Base Developable Photo-
 sensitive Polynorbornene **Mehrsa Raeis-Zadeh**
 Georgia Institute of
 Technology
- 2:45 - 3:10 **Break**

- 3:10 Ultra Low Temperature
 Curable Positive Tone
 Photodefineable
 Polybenzoxazole - II **Noritaka Matsuie**
 Yamazaki R&D Center,
 HD Microsystems, Ltd
 and Hitachi Chemical Co.
- 3:35 Underfill Material and
 Process Solution for Large
 Ultra Low K Flip Chip
 Encapsulation **Marie-Claude Paquet**
 IBM Bromont
- 4:00 Development of Thick
 Resist for Solder Bump **K. Mori**
 Yokkaichi Research Center,
 JSR Corporation
- 4:25 Reduced Warpage and
 Stress in Polymer Films for
 Microelectronics **Robert Hubbard**
 Lambda Technologies
- 5:30 - 7:00 **Symposium Reception - Reflecting Pool**

Wednesday **Session 2 - 3D/TSV/Novel Apps**
May 12, 2010

- 8:10 Direction of Microelectronics
 in Chip Packaging Technology **Eric Beyne**
 IMEC
- 8:55 Integration of Thinned Silicon
 Chips into a Polymer-Copper-
 Redistribution-A3-D Stacking
 Technology without TSVs **Tobias Baumgartner**
 Fraunhofer IZM
- 9:20 Evaluation of Photosensitive
 Spin-On Dielectrics for 3-D
 Wafer Level Packaging **F. Duval**
 IMEC, Leuven, Belgium
- 9:45 Coaxial Through Silicon Via
 for 3D Applications with
 Polyimide Dielectric **Richard Volant**
 IBM
- 10:10 - 10:35 **Break**
- 10:35 Electrografted Polymer Layers
 for Insulation of Deep TSV
 Structures **V. Mevellec**
 Alchimer SA
- 11:00 Implementation of 3D
 Lithography for Wafer Level
 Through Silicon Via (TSV)
 Applications **Alexander Feldman**
 Tessera
- 11:25 Temporary Wafer to Wafer
 bonding for 3D Integration
 using Polyimide Coatings **K. Zoschke**
 Fraunhofer Institute
- 11:50 Fabrication and Packaging of a
 Backside Contact, High Voltage
 Photovoltaic Device **Thomas Gorczyca**
 General Electric
- 12:15 - 1:30 **Lunch**
- 1:30 Wafer Level Via Filling and
 Interconnection Using
 Conductive Polymer by
 Screen Printing **Damien Saint-Patrice**
 CEA-LETI

- 1:55 Organic Optoelectronic
 Devices-Flexibility Versus
 Performance **Matt Aldissi**
 Fractal Systems
- 2:20 Novel Organosiloxane Polymers
 with Improved Device Properties **Edward W. Rutter, Jr.**
 Honeywell Electronic
 Materials

2:45 - 3:10 **Break**
Session 3 - Electronic Materials and Methods

- 3:10 Thermal Contact Materials
 Requirements for Testing of
 Electronic Packages **Ashish Gupta**
 Intel Corporation
- 3:35 Using High Temperature Thermal
 Conductivity to Assess Reliability/
 Performance of Epoxy Mold
 Compounds **Sheila Liza B. Dal**
 On Semiconductor
 Philippines Inc.
- 4:00 Printed Electronics-Fading into
 Reality **Donald Hayes**
 MicroFab Technologies,
 Inc.
- 4:25 Polymer Process Optimization
 Made Easy **Clifford J. Hamel**
 SUSS MicroTec, Inc.
- 6:00 - 9:30 **Exhibitors/Cocktails/ Dinner**

Thursday **Session 3 - Electronic Materials and Methods**
May 13, 2012

- 8:00 Electronic Packaging for
 High Performance Medical
 Imaging Systems **Bill Burdick**
 General Electric
- 8:45 Flexible Isotropically
 Conductive Adhesives with
 High Reliability and Mild
 Curing Condition **Dr. Cheng Yang**
 Department of
 Mechanical
 Engineering, The Hong
 Kong University
 of Science and
 Technology
- 9:10 Achieving Ceramic-like RF
 Capacitors Requirements with
 Organic based Materials **Jin-Hyun Hwang**
 Oak-Mitsui
 Technologies, LLC
- 9:35 Advanced Rework Solutions
 for Dielectric Film Removal
 in Semiconductor
 Manufacturing Processes **Diane Scheele**
 Dynaloy
- 10:00 - 10:25 **Break**
- 10:25 Preventing Reliability and
 Yield Degradations Caused
 by Bubble Defects **J. Braggin**
 Entegris
- 10:50 High Speed Shear Testing
 of WLCSP Solder Alloys,
 and the Correlation to JEDEC
 Board Drop Testing **Andrew J. Schoenberg**
 Fairchild Semiconductor
- 11:15 Packaging Requirements for
 Flexible CIGS **Todd Tolliver**
 GE Research